Claim 1 is amended as follows:

1. (Amended) A Dynamic Random Access Memory (DRAM), comprising:

a plurality of strip-type active areas on a substrate;

a plurality of shallow trench isolation regions on the substrate for isolating each of the active areas;

a plurality of word lines above the active areas and the shallow trench isolation regions, an array being formed by overlapping the word lines and the active areas, the array including a plurality of first overlapping portions and a plurality of second overlapping portions, wherein every two of the first overlapping portions are separated by every two of the second overlapping portions on each of the active areas and each of the first overlapping portions is next to each of the second overlapping portions on every two neighboring active areas; and

a capacitor array in the active areas, each of the capacitors being in each of the first overlapping portions, the capacitor including a deep trench structure and a collar isolation, a first collar portion being on an adjacent portion of two of the neighboring capacitors, a second collar portion being on a non-adjacent portion of two of the neighboring capacitors, the first collar portion being longer than the second collar portion in a depth direction of the deep trench and a depth of the second collar portion being the same as a depth of the top plate, wherein a memory cell is formed by the word line in one of the second overlapping portions and the capacitor in one of the first overlapping portions.

Add the following new claims:

36. (New) A deep trench capacitor for Dynamic Random Access Memory (DRAM), comprises:

a deep trench structure;

a bottom plate on an interface region of the substrate and a lower sidewall portion of the deep trench structure;

a dielectric layer, formed on an internal surface of the bottom plate;

a top plate, formed by filling the deep trench structure and covering the dielectric layer with a conductive material;

a first collar portion being on an adjacent portion of two of the neighboring capacitors;

a second collar portion being on a non-adjacent portion of two of the neighboring capacitors, wherein the first collar portion being longer than the second collar portion in a depth direction of the deep trench; and

a buried strap conductive layer, above the second collar portion.

37. (New) The deep trench capacitor as recited in claim 36, wherein the bottom plate is formed by thermal diffusion with an impurity gas to dope the lower sidewall portion of the deep trench structure.

38. (New) The deep trench capacitor as recited in claim 36, wherein the top plate comprises a polysilicon layer doped with arsenic.

39. (New) The deep trench capacitor as recited in claim 36, wherein a depth of the second collar portion being the same as a depth of the top plate.

40. (New) The deep trench capacitor as recited in claim 36, wherein a thickness of the first collar portion and the second collar portion is about 400Å-500Å for respectively isolating the neighboring capacitors and sufficiently decreasing a leakage current of the substrate theresurrounding.

41. (New) The deep trench capacitor as recited in claim 36, wherein the capacitor further comprises:

a trench top isolation, above the buried strap conductive layer, wherein the trench top isolation connects with the shallow trench isolation regions in a word line direction.

42. (New) The deep trench capacitor as recited in claim 36, wherein the buried strap conductive layer further comprises a doped silicon layer and the diffusion conductive region is formed by a thermal process on the doped silicon layer.

43. (New) The deep trench capacitor as recited in claim 41, wherein the trench top isolation further comprises a silicon oxide layer.

44. (New) The deep trench capacitor as recited in claim 41, wherein the shallow trench isolation regions further comprises a silicon oxide layer.

45. (New) The deep trench capacitor as recited in claim 36, wherein the buried strap conductive layer including a diffusion conductive region in the substrate outside the buried strap conductive layer